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STERNE, KESSLER, GOLDSTEIN & FOX P.L.L.C.
1100 NEW YORK AVENUE, N.W.
WASHINGTON, DC 20005

EXAMINER	
DO, CHAT C	

ART UNIT	PAPER NUMBER
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

MN

Office Action Summary	Application No.	Applicant(s)	
	09/788,670	EKNER ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 May 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *43-81* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *43-81* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This communication is responsive to Amendment filed 05/29/2007.

2. Claims 43-81 are pending in this application. Claims 43, 55, and 69 are independent claims. In Amendment, claims 1-42 are previously cancelled. This Office Action is made non-final after a RCE filed 05/29/2007.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 43-81 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claims 43-81 cite a processor, medium, and system for performing structure multiplication in accordance with a mathematical algorithm. In order for claims to be statutory, claims must either include a practical/physical application. However, claims 43-81 merely disclose steps/components for performing structure multiplication without further disclosing a practical/physical application or a useful and tangible result since the claims appear to preempt every substantial practical application of the idea embodied by the claim and there is no cited limitation in the claims that breathes sufficient life and meaning into the preamble so as to limit it to a particular practical application rather than being so broad and sweeping as to cover every substantial practical application of the

idea embodied therein. Further, claims 55-68 are software per se since the medium comprising a processor is embodied in software. Therefore, claims 43-81 are directed to non-statutory subject matter.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 43, 50-55, 62-66, 69, and 76-81 are rejected under 35 U.S.C. 103(a) as being obvious over Choquette (U.S. 6,480,872) in view of Glaser et al. (U.S. 6,397,241).

Re claim 43, Choquette discloses in Figure 4 a processor (e.g. abstract and Figure 4 component 400) comprising: a first array that is used to perform arithmetic multiplication (e.g. 410), the first array having a first result output and a second result output (e.g. C and S result from 410); and a carry propagation adder having a first input and a second input (e.g. adder 512 with all the inputs into the adder), wherein the first input of the carry propagation adder is coupled to the first result output of the first array, and the second input of the carry propagation adder is coupled to the second result output of the first array (e.g. adder 512). Choquette fails to disclose in Figure 4 a second array that is used to perform binary polynomial multiplication, the second array having a third result output and it connects to the adder. However, Glaser et al. disclose in Figures 3-5 a second array that is used to perform binary polynomial multiplication, the second array

having a third result output and it connects to the adder (e.g. abstract, Figures 3-5, col. 2 lines 1-10, col. 3 lines 36-44, and col. 5 lines 50-60). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second array that is used to perform binary polynomial multiplication, the second array having a third result output and it connects to the adder as seen in Glaser et al.'s invention into Choquette's invention because it would enable to perform multiplication in Galois field (e.g. col. 2 lines 1-10).

Re claim 50, Choquette further discloses in Figure 4 the first array is a 32-bit by 16-bit array (e.g. the first operand can be 32 in size in col. 4 lines 45-65).

Re claim 51, Choquette fails to disclose the second array is a 32-bit by 16-bit array. However, Glaser et al. disclose the second array is a 32-bit by 16-bit array (e.g. col. 5 lines 50-60 any size). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add a second array is a 32-bit by 16-bit array as seen in Glaser et al.'s invention into Choquette's invention because it would enable to perform multiplication in Galois field (e.g. col. 2 lines 1-10).

Re claim 52, Choquette further discloses in Figure 4 the processor performs 32-bit by 32-bit multiplication (e.g. the first operand can be 32 in size in col. 4 lines 45-65).

Re claim 53, Choquette further discloses in Figure 4 the processor multiplies a first operand and second operand to form a resultant value (e.g. A and B as input operands the CS as output resultant), the first operand being provided to a first input of the first array and the second operand being provided to a second input of the first array,

and wherein the resultant value is available at an output of the carry propagation adder (e.g. CS are fed directly to the adder 512).

Re claim 54, Choquette fails to disclose in Figure 4 the processor multiplies a polynomial first operand and second polynomial operand to form a resultant value, the first polynomial operand being provided to a first input of the second array and the second polynomial operand being provided to a second input of the second array, and wherein the resultant value is available at an output of the carry propagation adder. However, Glaser et al. disclose in Figures 3-5 the processor multiplies a polynomial first operand and second polynomial operand to form a resultant value, the first polynomial operand being provided to a first input of the second array and the second polynomial operand being provided to a second input of the second array, and wherein the resultant value is available at an output of the carry propagation adder (e.g. the input operands is A and B and the output is P as seen in col. 3 lines 36-44). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the processor multiplies a polynomial first operand and second polynomial operand to form a resultant value, the first polynomial operand being provided to a first input of the second array and the second polynomial operand being provided to a second input of the second array, and wherein the resultant value is available at an output of the carry propagation adder as seen in Glaser et al.'s invention into Choquette's invention because it would enable to perform multiplication in Galois field (e.g. col. 2 lines 1-10).

Re claim 55, it is a computer-readable medium claim of claim 43. Thus, claim 55 is also rejected under the same rationale as cited in the rejection of rejected claim 43.

Re claim 62, it is a computer-readable medium claim of claim 50. Thus, claim 62 is also rejected under the same rationale as cited in the rejection of rejected claim 50.

Re claim 63, it is a computer-readable medium claim of claim 51. Thus, claim 63 is also rejected under the same rationale as cited in the rejection of rejected claim 51.

Re claim 64, it is a computer-readable medium claim of claim 52. Thus, claim 64 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

Re claim 65, it is a computer-readable medium claim of claim 53. Thus, claim 65 is also rejected under the same rationale as cited in the rejection of rejected claim 53.

Re claim 66, it is a computer-readable medium claim of claim 54. Thus, claim 66 is also rejected under the same rationale as cited in the rejection of rejected claim 54.

Re claim 69, it is a system claim of claim 43. Thus, claim 69 is also rejected under the same rationale as cited in the rejection of rejected claim 43.

Re claim 76, it is a system claim of claim 50. Thus, claim 76 is also rejected under the same rationale as cited in the rejection of rejected claim 50.

Re claim 77, it is a system claim of claim 51. Thus, claim 77 is also rejected under the same rationale as cited in the rejection of rejected claim 51.

Re claim 78, it is a system claim of claim 52. Thus, claim 78 is also rejected under the same rationale as cited in the rejection of rejected claim 52.

Re claim 79, it is a system claim of claim 53. Thus, claim 79 is also rejected under the same rationale as cited in the rejection of rejected claim 53.

Re claim 80, it is a system claim of claim 54. Thus, claim 80 is also rejected under the same rationale as cited in the rejection of rejected claim 54.

Re claim 81, Choquette further discloses in Figure 4 operation of the multiply-divided unit is decoupled from operation of the execution unit (e.g. 116 in Figure 1).

7. Claims 48-49, 60-61, and 74-75 are rejected under 35 U.S.C. 103(a) as being obvious over Choquette (U.S. 6,480,872) in view of Glaser et al. (U.S. 6,397,241), as applied to claims 43, 55, and 69 respectively, in further view of Bhandal et al. (U.S. 6,711,602).

Re claims 48-49, Choquette in view of Glaser et al. fail to disclose in Figure 4 the first array includes a plurality of carry-save adders arranged in a Wallace tree structure array. However, Bhandal et al disclose in Figures 5-8 the arithmetic multiplier includes a Wallace tree multiplier array (e.g. all levels of CSA in Figure 7). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the arithmetic multiplier includes a Wallace tree multiplier array as seen in Bhandal et al.'s invention into Choquette in view of Glaser et al.'s invention because it would enable to reduce the circuitry complexity and increase the system performance in performing multiplication.

Re claim 60, it is a computer-readable medium claim of claim 48. Thus, claim 60 is also rejected under the same rationale as cited in the rejection of rejected claim 48.

Re claim 61, it is a computer-readable medium claim of claim 49. Thus, claim 61 is also rejected under the same rationale as cited in the rejection of rejected claim 49.

Re claim 74, it is a system claim of claim 48. Thus, claim 74 is also rejected under the same rationale as cited in the rejection of rejected claim 48.

Re claim 75, it is a system claim of claim 49. Thus, claim 75 is also rejected under the same rationale as cited in the rejection of rejected claim 49.

8. Claims 67-68 are rejected under 35 U.S.C. 103(a) as being obvious over Choquette (U.S. 6,480,872) in view of Glaser et al. (U.S. 6,397,241), as applied to claim 43, 55, and 69 respectively, in further view of Bair et al. (U.S. 6,066,178).

Re claims 67-68, Choquette in view of Glaser et al. fail to disclose the processor is embodied in hardware description language software wherein the language is one of Verilog hardware description language software and VHDL hardware description language software. However, Bair et al. disclose the processor is embodied in hardware description language software wherein the language is one of Verilog hardware description language software and VHDL hardware description language software (e.g. col. 3 lines 50-65). Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention is made to add the processor is embodied in hardware description language software wherein the language is one of Verilog hardware description language software and VHDL hardware description language software as seen in Bair et al.'s invention into Choquette in view of Glaser et al.'s invention because it would enable to automate design and synthesis of a digital multiplier in hardware (e.g. col. 1 lines 5-10).

Response to Arguments

9. Applicant's arguments with respect to claims 43-81 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

August 6, 2007